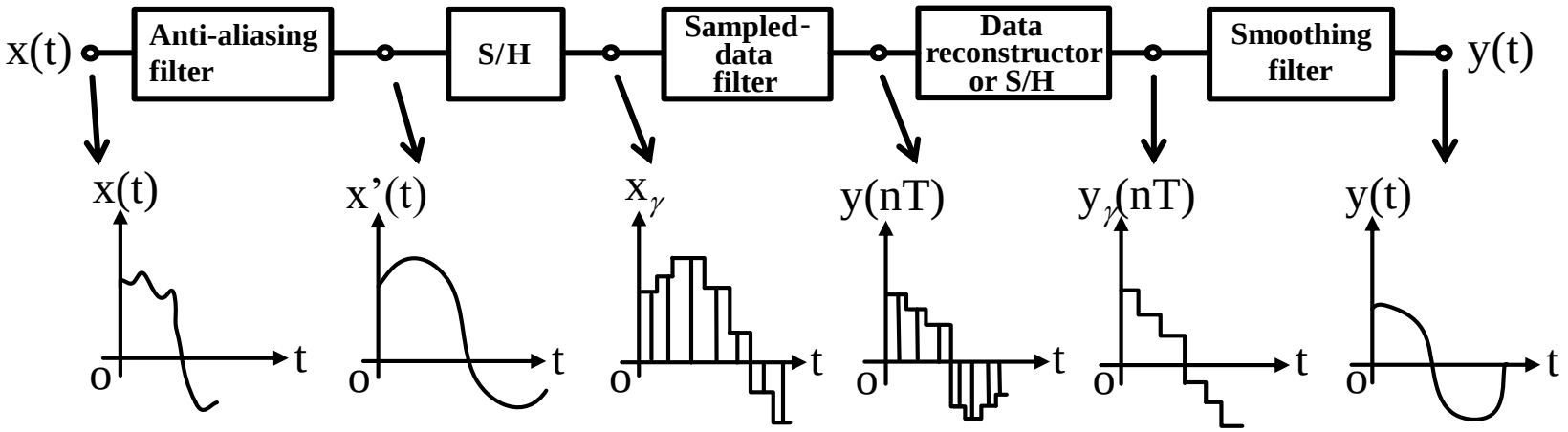
Introduction to Semiconductor

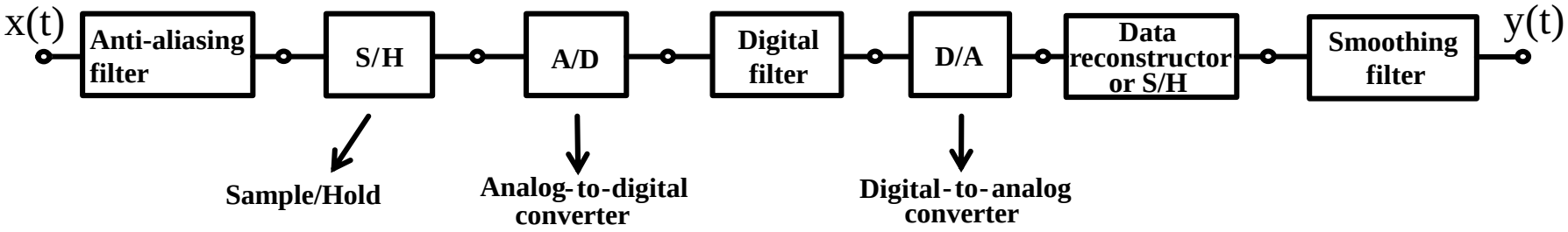
Signal Processing (Example: Filtering Path)

- With analog filter (before 1980)

- With sampled data filter (1980s)



- With digital filter (after 1990)



Analog Systems

- A/D converters
  - Serial ADC, successive approximation ADC, Parallel ADC, Self-calibrating ADC, Pipeline ADC, Oversampled and/or delta-sigma ADC (Z-domain)
- D/A converters
  - Current-scaling DAC, serial DAC, Voltage-scaling DAC, Delta-sigma DAC, Charge-scaling DAC, DAC using combinations of scaling approaches
- Continuous-time filters
  - Low pass filter, BPF,HPF,…
- Switched-capacitor filter and digital filters
- Modulators and Multipliers
- Oscillators and Phase-locked loops
- DC/DC converter
  - Switched-inductor
  - Switched-capacitor
  - Analog and digital low dropout (LDO) regulator
- Wireless power transfer
- Energy harvesting
- Others

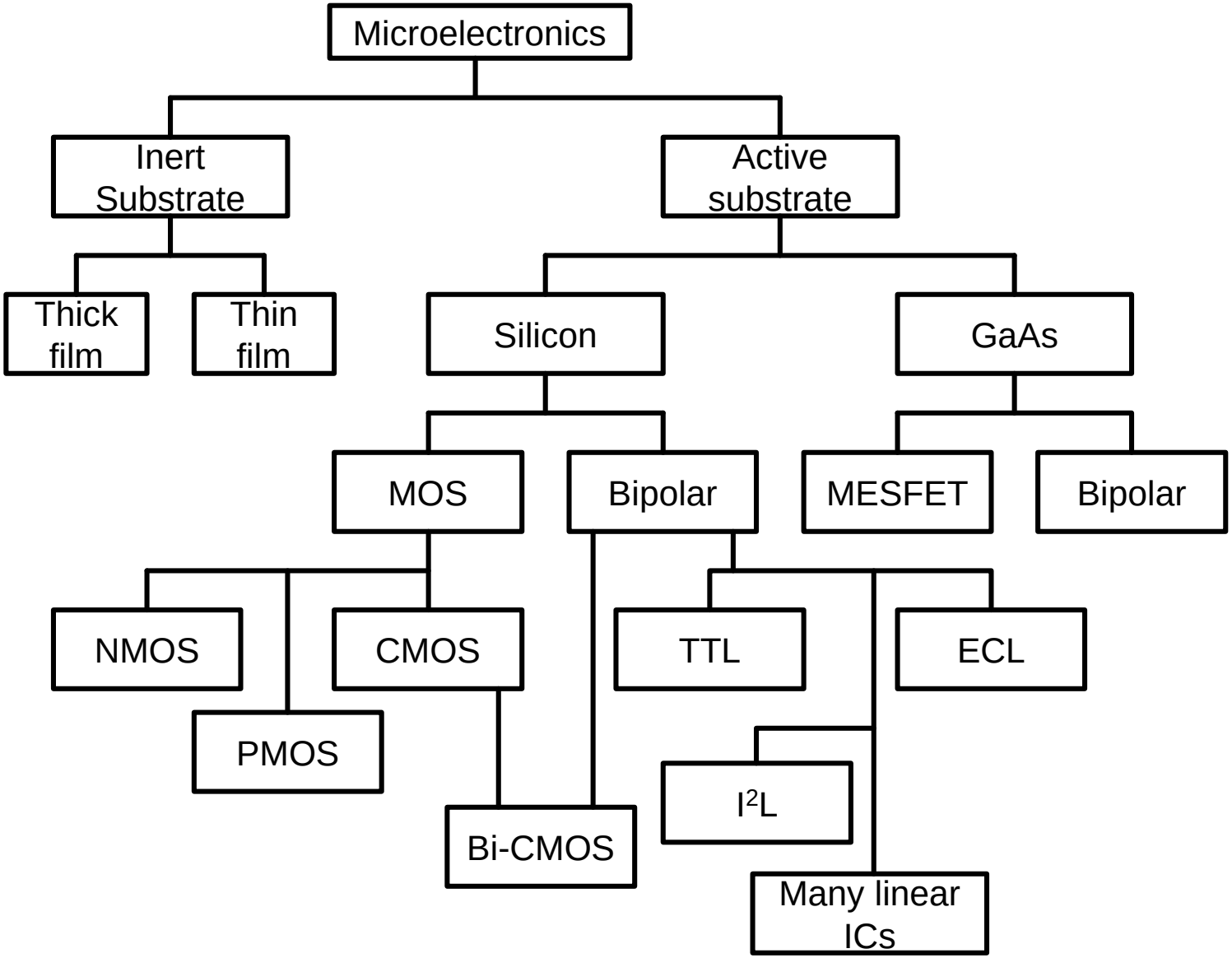
Basic Integrated Building Blocks of Analog Systems

- Switches
- Active Resistors
- Current Sources and Sinks
- Current Mirrors
- Voltage and Current References
- Operational Amplifiers
- Digital Circuits
- Others

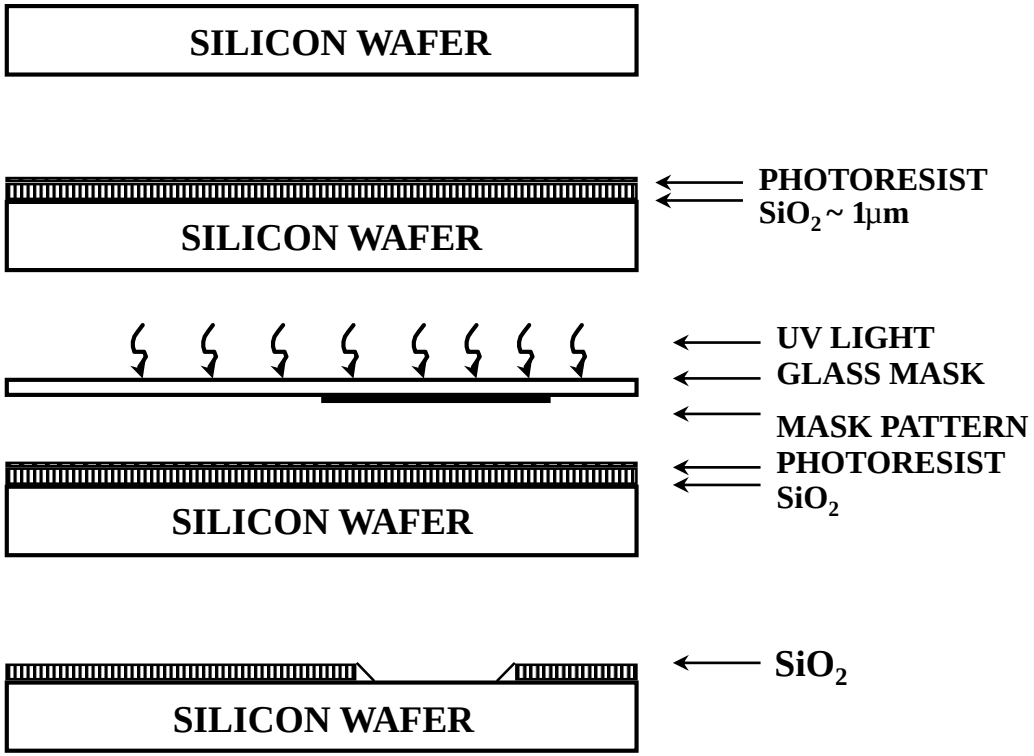
Devices and Technologies

- Devices
  - MOSFETs: NMOS and PMOS
  - Bipolar Transistors: NPN and PNP
  - MESFETs: N-type and P-type
  - Diode/Zener
  - Resistor
  - Capacitor
  - Others
- Technologies
  - CMOS
  - Bipolar
  - BiCMOS
  - GaAs
  - Others

Major Process Used in IC Fabrication



MOS Fabrication

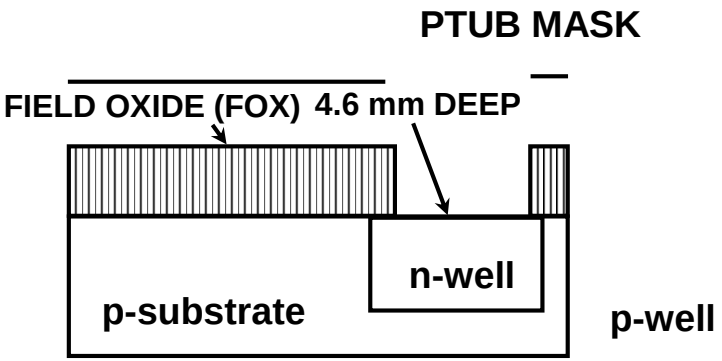


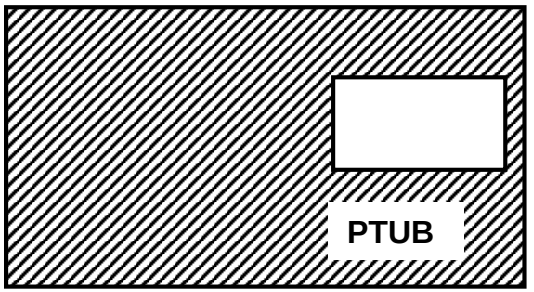
- Photoresists
  - NEG - first historically
  - POS - better for dimensions < 2.5um
  - NEG - insoluble where exposed
  - POS - soluble where exposed

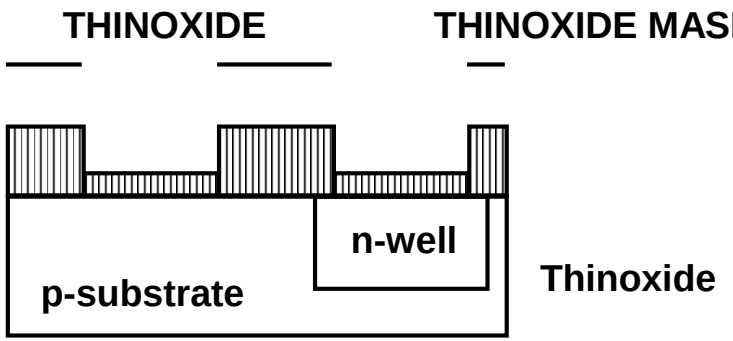
CMOS N-Well Process Flow

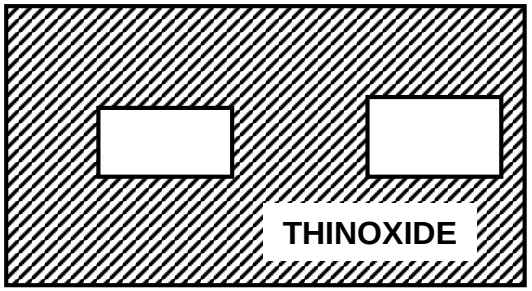
Cross section of physical structure (side View)

Mask (Top View)

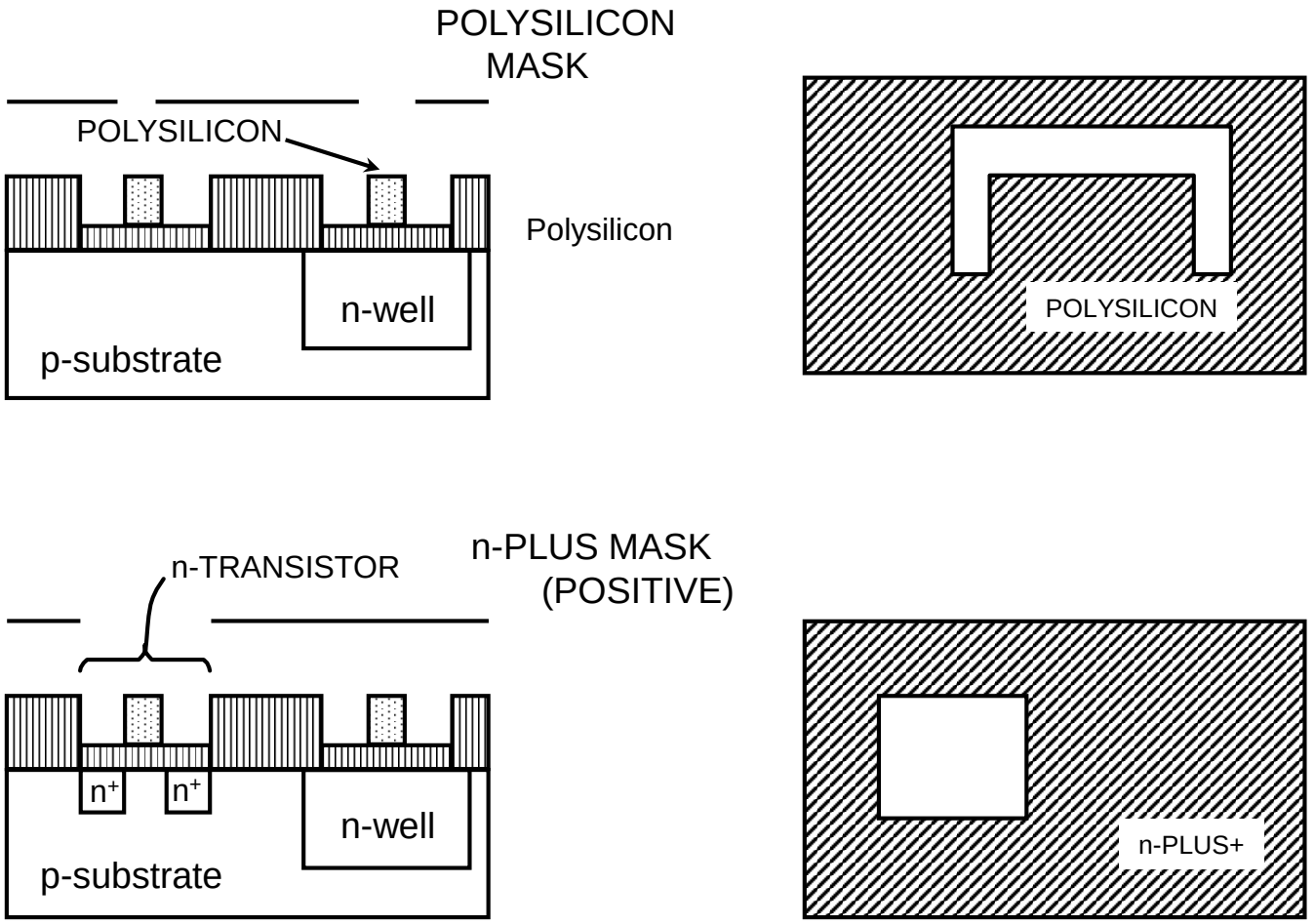




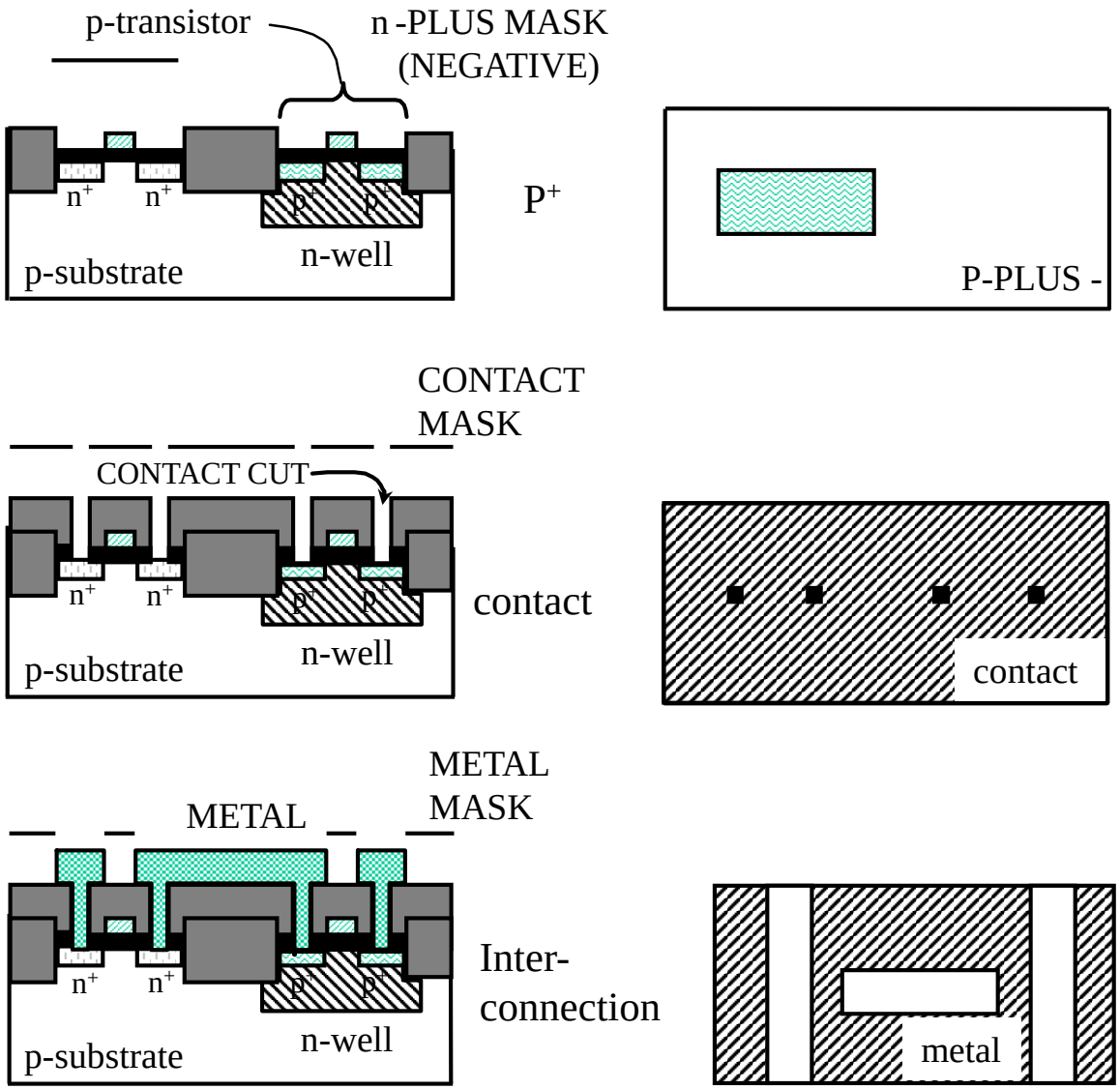




CMOS N-Well Process Flow (Cont.)

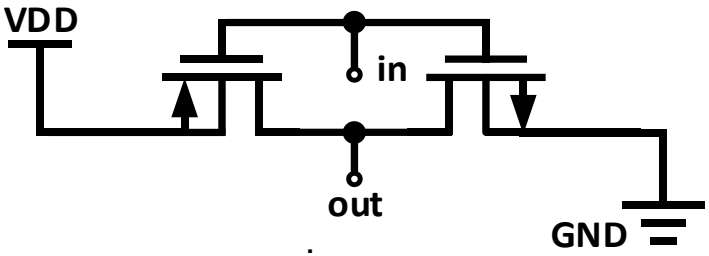


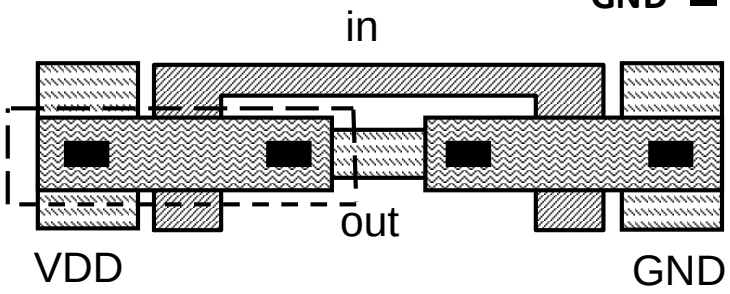
CMOS N-Well Process Flow (Cont.)

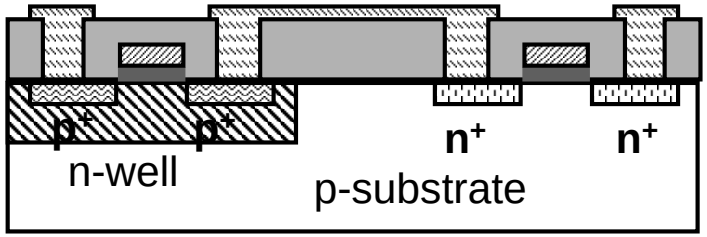


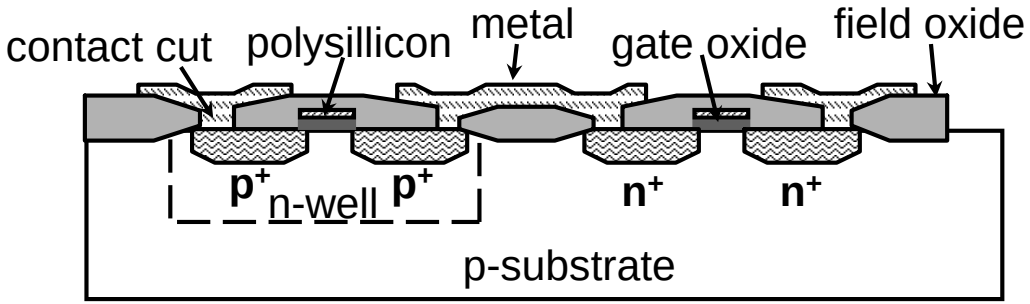
Cross Section of a CMOS Inverter

- N-well process



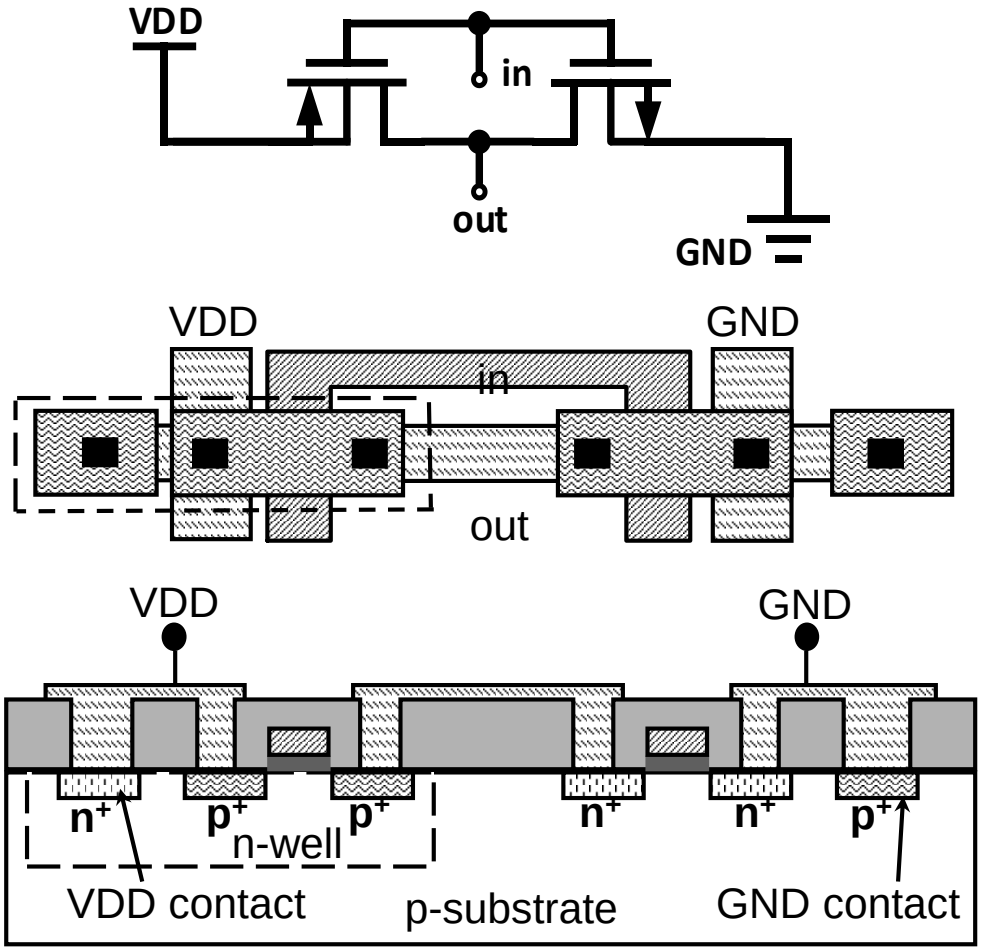






Cross Section of a CMOS Inverter(Cont.)

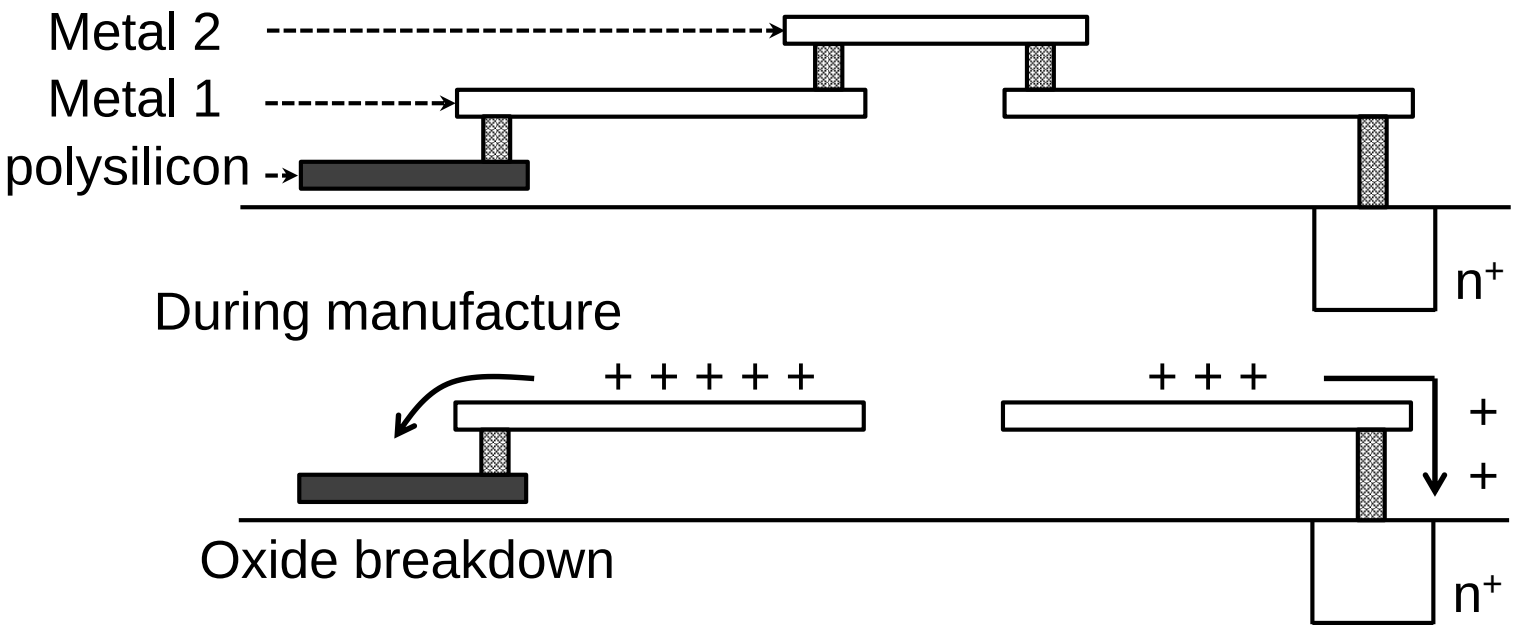
- With substrate contact



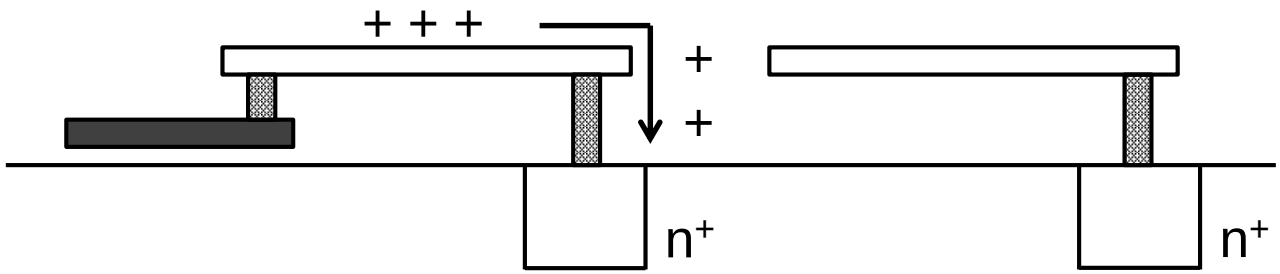
- P-well process can be similarly obtained

Antenna Rule

- Device may be damaged by static charges that develop on conductors during manufacture



- If the path is too long, we can arrange a discharge path as the following drawing



Classification of Integrated Circuits by Device Count

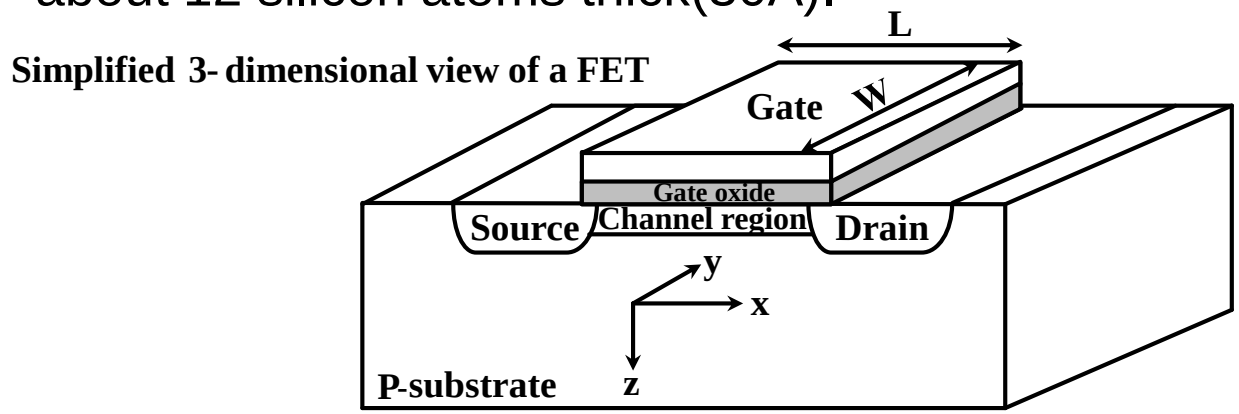
Nomenclature	Abbr.	Active Device Count	Typical Functions
Small-Scale Integration	SSI	1-100	Gates, Opamps, Many linear applications
Medium-Scale Integration	MSI	100-1,000	Registers, Filters, etc.
Large-scale Integration	LSI	1,000-100,000	Microprocessors, A/D, etc.
Very Large-scale Integration	VLSI	>100,000	Memories, Computers, Signal Processors

Conversion of parameters used for device characterization in semiconductor industry

Unit	Symbol	Femto	Pico	Angstroms	Nano	Microns	Mils	Meters	Inches
Femto	f	–	10^{-3}p	10^{-5}	10^{-6}n	10^{-9}μ	3.94×10^{-11}mil	10^{-15}m	3.94×10^{-14}in
Pico	p	10^{3}f	–	10^{-2}	10^{-3}n	10^{-6}μ	3.94×10^{-8}mil	10^{-12}m	3.94×10^{-11}in
Angstroms	Å	10^{5}f	10^{2}p	–	10^{-1}n	10^{-4}μ	3.94×10^{-6}mil	10^{-10}m	3.94×10^{-9}in
Nano	n	10^{6}f	10^{3}p	10^{1}Å	–	10^{-3}μ	3.94×10^{-5}mil	10^{-9}m	3.94×10^{-8}in
Micron	μ	10^{9}f	10^{6}p	10^{4}Å	10^{3}n	–	0.0394mil	10^{-6}m	3.94×10^{-5}in
Mil	mil	2.54×10^{10}f	2.54×10^{7}p	2.54×10^{5}Å	2.54×10^{4}n	25.4 μ	–	2.54×10^{-5}m	0.001 in
Meter	m	10^{15}f	10^{12}p	10^{10} Å	10^{9}n	10^{6}μ	3.9×10^{4}mil	–	39 in
Inch	in	2.54×10^{13}f	2.54×10^{10}p	2.54×10^{8}Å	25.4×10^{6}n	25.4×10^{3}μ	10^{3}mil	2.54×10^{-2}m	–

Minimum Feature size

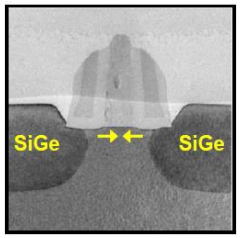
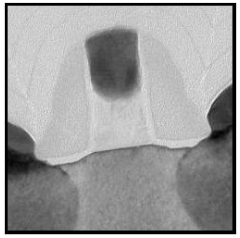
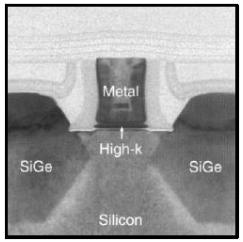
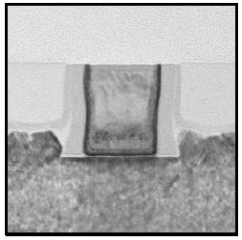
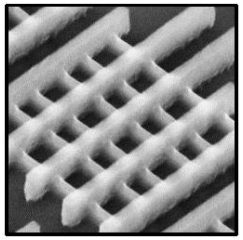
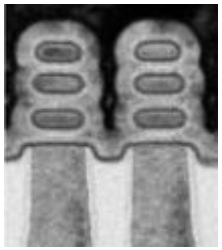
- Min. feature size ≈ min. allowable value for L
  - In a 90nm process, the minimum permissible value of L would be 90nm and W would be 90nm.
  - The area required for the gate of the transistor in such a process would be 0.0081μm^2.
- The vertical dimensions are typically much smaller than the lateral dimensions
  - The thin insulating layer under the gate in a typical 90nm process is about 12 silicon atoms thick(30Å).



- Feature size, 0.5μm, 0.35μm, 0.25μm, 0.18μm, 0.13μm, 90nm, 65nm, 45nm, 28nm, 20nm, 14nm, 10nm, 7nm ,5nm, 3nm, 2nm …etc.

Semiconductor Process Evolution

- CMOS process evolution

Year	2003	2005	2007	2009	2011	?
Micro-photo						
Process	90 nm	65 nm	45nm	32 nm	22 nm	? nm
Equivalent gate oxide Thickness (EOT)	12 Å (SiO_2) < $5T_{Si}$	12 Å (SiO_2) < $5T_{Si}$	10 Å (HfO_2) < $4T_{Si}$	9 Å (HfO_2) < $4T_{Si}$	5 Å (?) < $2T_{Si}$	?
Technology	SiGe Strained silicon	High-k + metal gate	Tri-gate	Gate-all-around		

*T_{si}: Silicon atoms thickness ≈ 2.7Å , $k_{SiO2}=3.9\varepsilon_0$, $k_{HfO2}=25\varepsilon_0$ $*\mathrm{EOT} = t_{high-k}\left(k_{SiO_2}/k_{high-k}\right)$

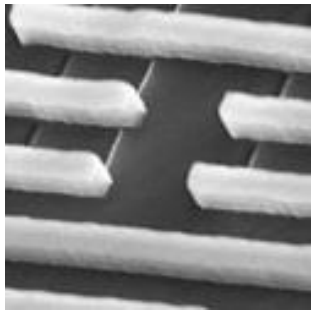
- Strained silicon: Energy band changed → Electron mobility ↑
- High-k + metal gate: Increasing C_{OX} and reducing tunneling current
- Tri-gate: Needed to continue Moore's Law

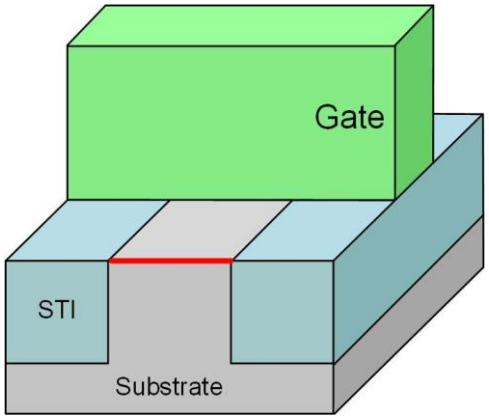
Source: Intel, IBM

Introduction of Tri-gate and GAA Transistor

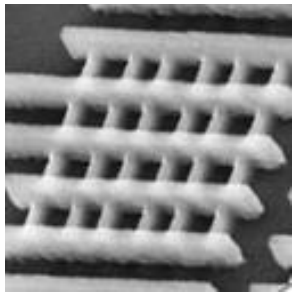
- Similar Tri-gate concept used by TSMC is FinFET

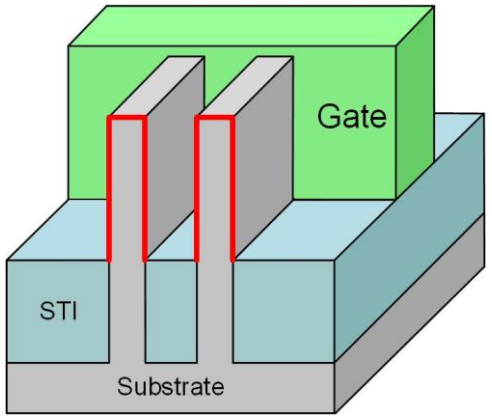
- Planar transistor (Intel 32nm)



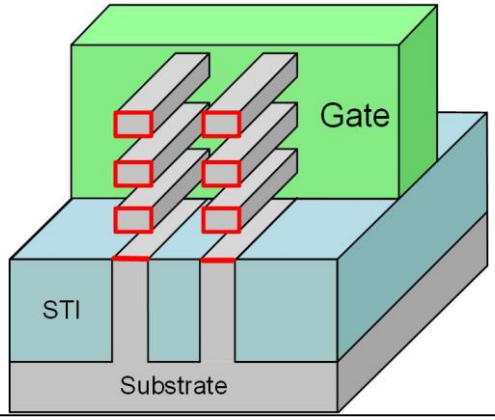


- Tri-gate transistor (Intel 22nm)





- Gate-all-around (GAA) transistor (IBM 5nm)

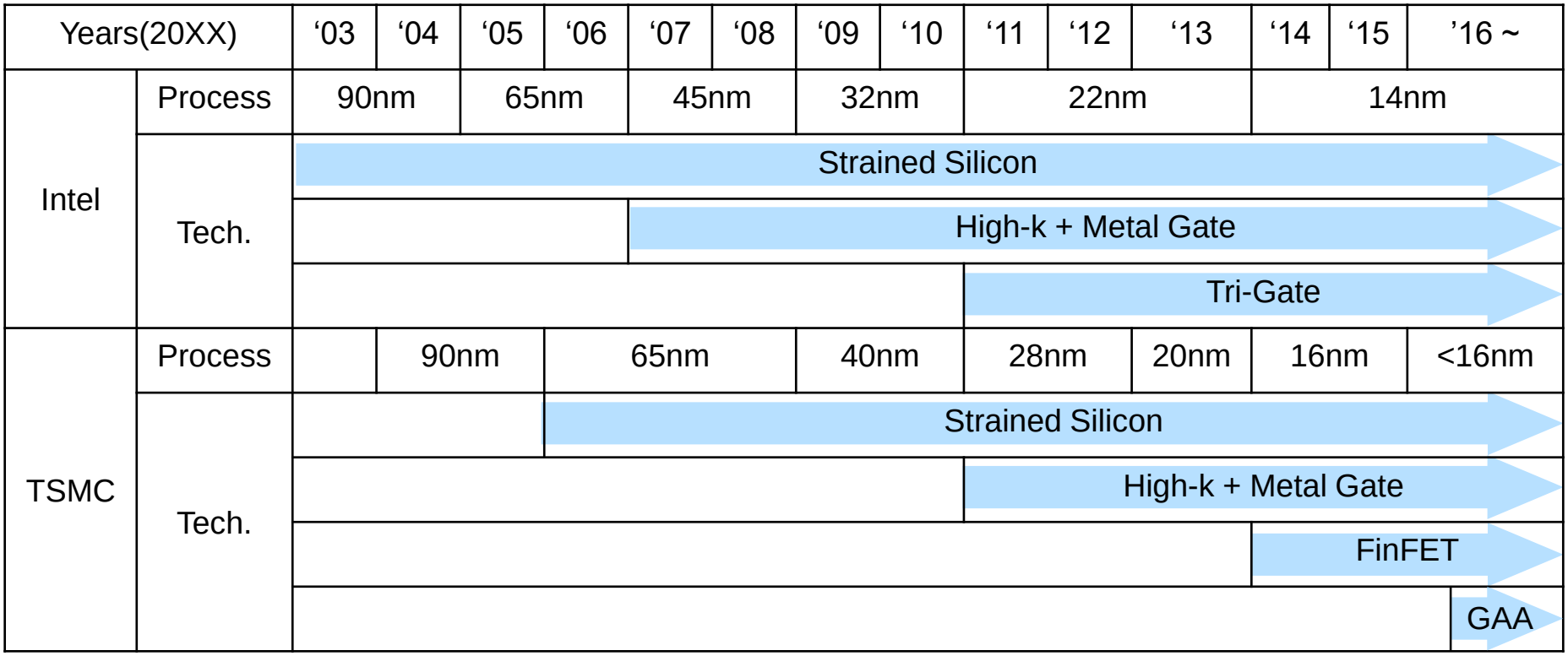


Effective width

Source: Intel, IBM

Comparison between TSMC and Intel Process

- Process roadmap of TSMC and Intel



TSMC GAA will be used for 2nm process in 2025.

Evolution of Design Rules

- Category
  - Design rule check (DRC)
  - Design for Manufacturability (DFM) (Only for process < 130nm)
  - Antenna rule
- Number of typical process rules

	Number of rules		
Process	DRC + DFM	Antenna	Total
350nm	<200	<10	~250
250nm (HV)*	<1000	<50	~1100
180nm	<500	<50	~600
90nm	<1500	N/A	~1500
40nm	<2500	N/A	~2500
28nm	<3500	<150	~4000
16nm	<8000	<150	~8000

*: High-voltage

Transistor Count

- For a 12in wafer with 90nm x 90nm transistor, its transistor count

$$N_{90nm} = \frac{\pi(6in)^2}{n \times (90nm)^2} \cdot \left(\frac{2.54 \times 10^7 nm}{in} \right)^2 = 9.0 \times 10^{11}$$

where n ≈ 10 due to drain, source area, routing areas and layout spacing

- The impact of shrinking the feature size can now be appreciated. If we could build transistor gate that were 3nm x 3nm,the number of transistors that could be accommodated by the same 12 inch wafer in the 3nm process becomes

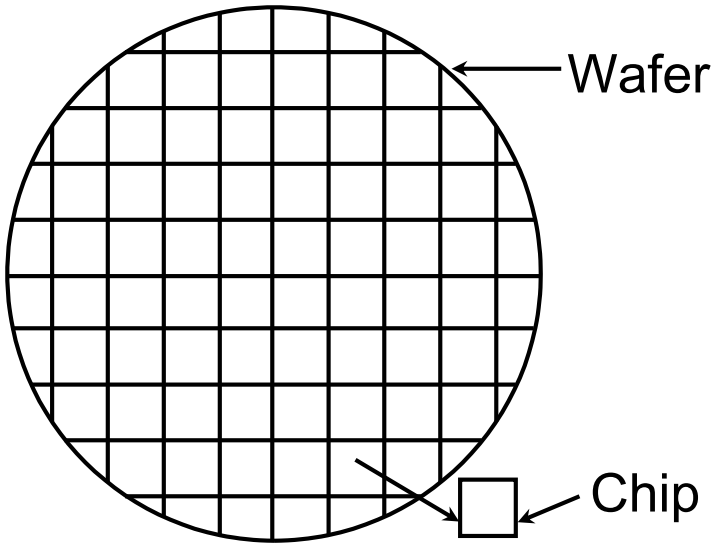
$$N_{3nm} = \frac{\pi(6in)^2}{n \times (3nm)^2} \cdot \left(\frac{2.54 \times 10^7 nm}{in} \right)^2 = 8.1 \times 10^{14}$$

where n ≈ 10 due to drain, source area, routing areas and layout spacing. In 3 cm^2 active area, there are 3.3 trillion transistors!

- Subject to the same reduction for spacing and interconnections as in the 90nm process. Nonetheless, the 1000-fold increase in device count is very significant

Sketch of Wafer Showing Repeated “Chips”

- TI 16-Mbit DRAM (1991)
  - Fabricated in a 0.6μm process with a die area of 1 cm^2
  - It has 16,770,000 transistors and 16,770,000 capacitors in memory array, along with over 150,000 transistors in the control circuit
- Another company 16-Gbyte DRAM (2018)
  - Fabricated in a 20 nm-class process with a die area of 1 cm^2
  - It has 137,438,953,472 transistors and 137,438,953,472 capacitors in memory array, along with over 1,000,000 transistors in the control circuit



Note : 20nm-class means a process technology node somewhere between 20 and 29 nanometers.

Economics

- Major costs associated with wafer processing and fabrication
- Process(1988) based upon volume production
- Processing cost of wafer fabrication

	Processing Cost		
	Evaluation	4” Process	5” Process
Blank Wafer	Per Wafer	$10	$15
Wafer Processing	Per Wafer	$140	$150
Wafer Probe	Per Wafer	$25	$40
Wafer Sawing	Per Wafer	$3	$3
Die Attach and Bonding	Per Wafer	$3	$5
Packaging	Per Die	Next page	Next page
Final Test	Per Package	$30/cm^2	$30/cm^2

Economics (Cont.)

1980s Package costs		
Plastic DIP	8pin	$0.032
Plastic DIP	16pin	$0.048
0.048Plastic DIP	24pin	$0.091
Plastic DIP	64pin	$0.70
Ceramic side brazed	16pin	$1.05
Ceramic side brazed	24pin	$1.50
Ceramic side brazed	64pin	$4.95
Ceramic CERDIP	16pin	$0.096
Ceramic CERDIP	24pin	$0.26
Ceramic CERDIP	40pin	$0.64
Ceramic pin grid array	68pin	$6.40
Ceramic pin grid array	84pin	$7.50
Ceramic pin grid array	132pin	$10.15
Ceramic pin grid array	224pin	$18.00

Foundry Sale Price Per Chip in 2020

- Calculation of foundry sale price per chip in 2020 by node

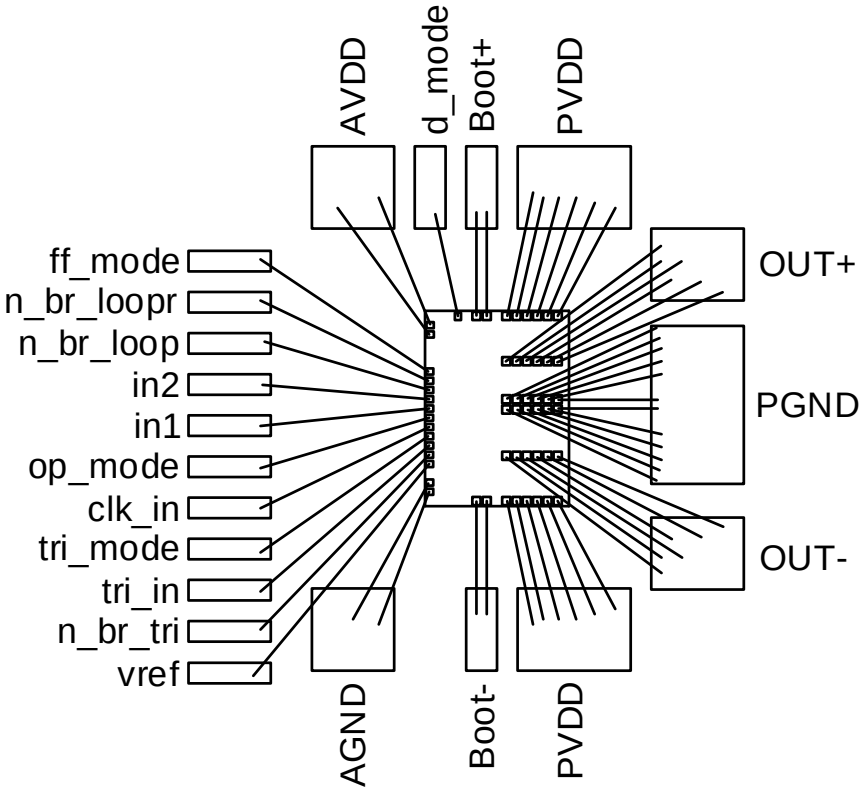
Node (nm)	90	65	40	28	20	16/12	10	7	5
Mass production year and quarter 量產年份和季度	2004 Q4	2006 Q4	2009 Q1	2011 Q4	2014 Q3	2015 Q3	2017 Q2	2018 Q3	2020 Q1
Foundry sale price per wafer (USD) 每個晶圓的代工銷售價格	1,650	1,937	2,274	2,891	3,677	3,984	5,992	9,346	16,988
Foundry sale price per chip (USD) 每個晶片的代工銷售價格 (附註)	2,433	1,428	713	453	399	331	274	233	238

附註: 以晶片在相同功能與規格條件下計算(以Nvidia's Tesla P100 GPU為例)

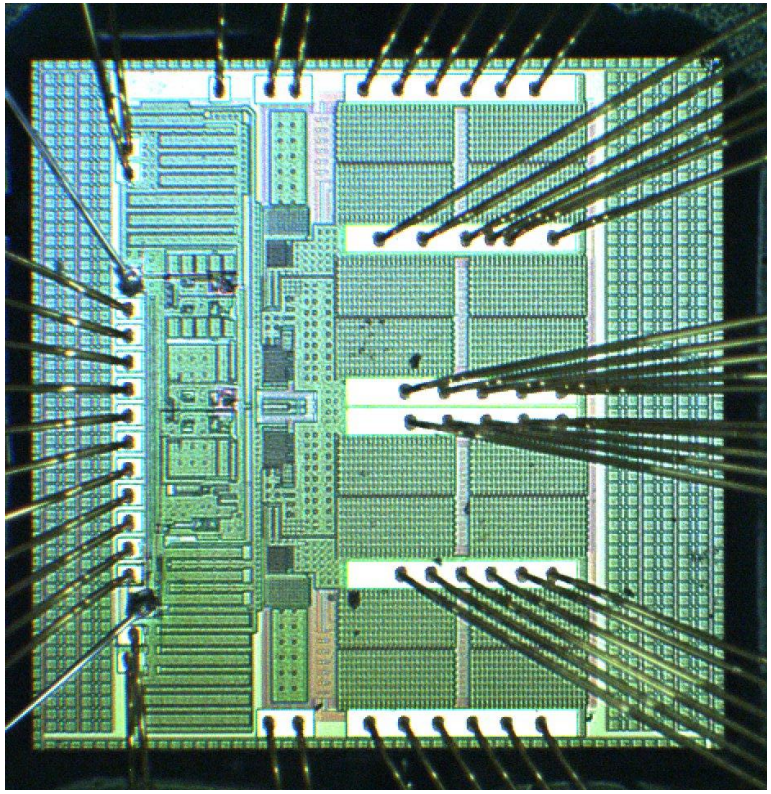
轉載自: https://cset.georgetown.edu/publication/ai-chips-what-they-are-and-why-they-matter/

Packaged IC

- Bonding diagram and floorplan

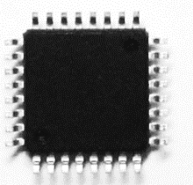


- Die photo with bonding wires



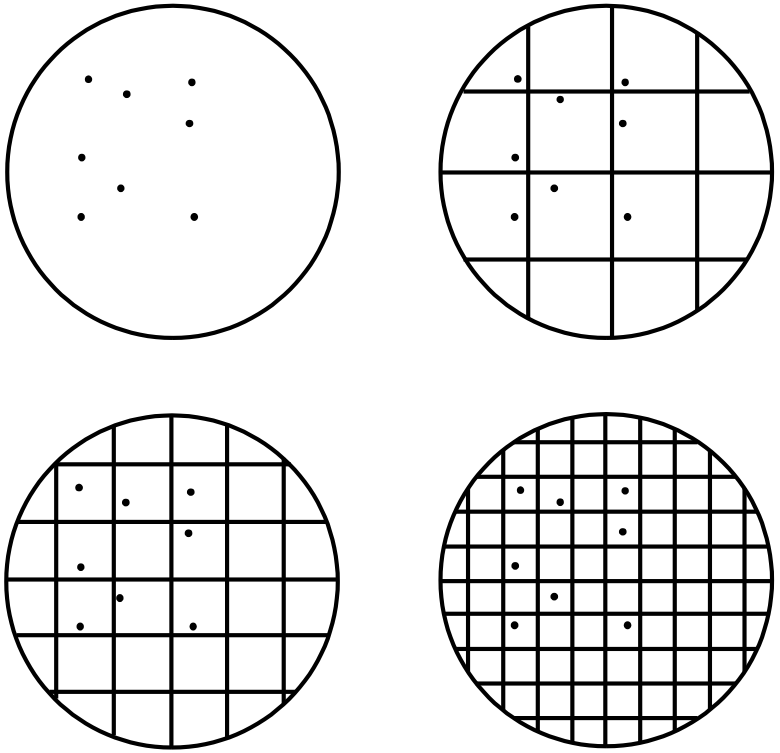
- Packaged IC

Front 

Back 

Yield

- Defect effect



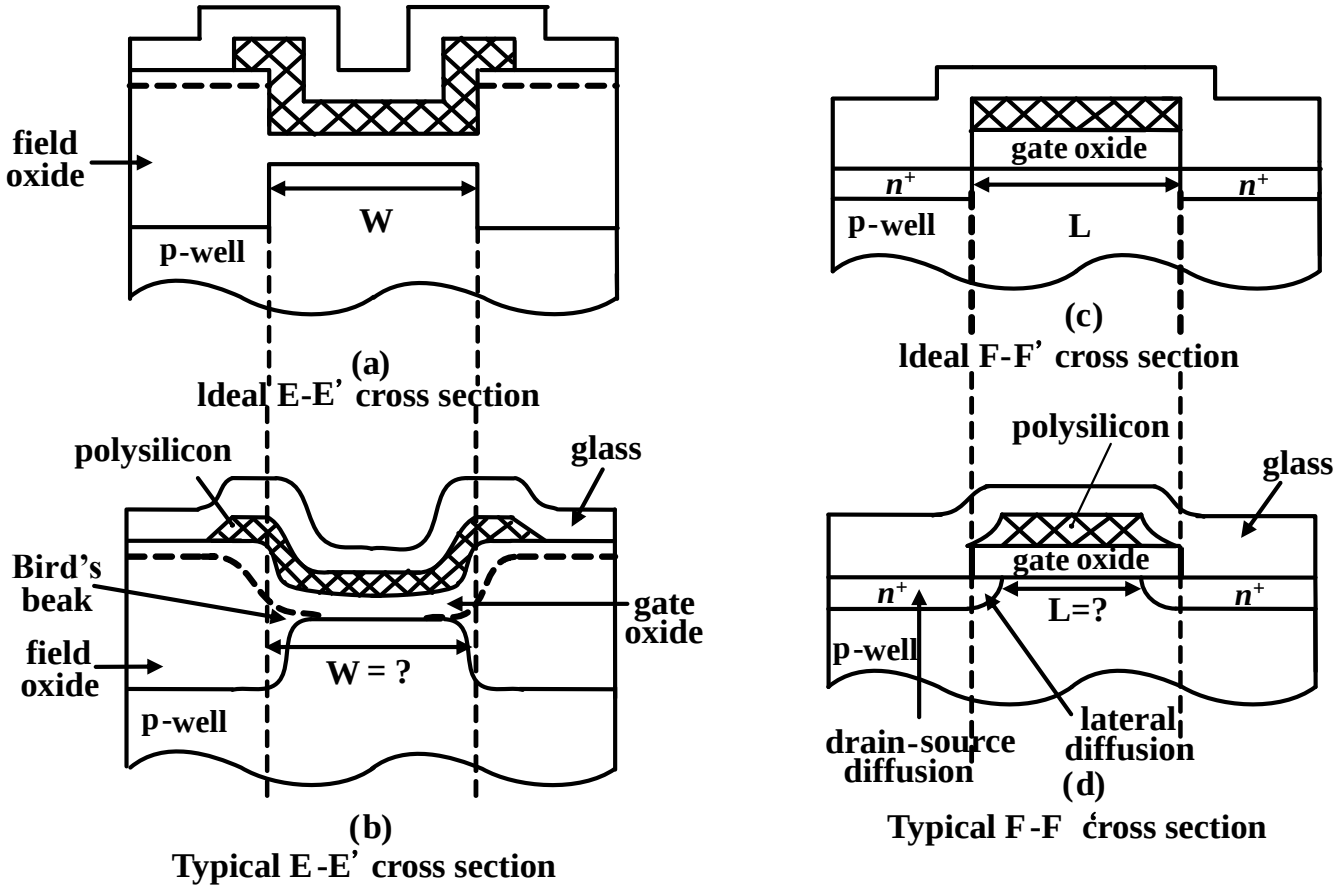
- Probability that a die is good , P
  - P is a function of A&D
  - A: die area
  - D: defect density

e.g. $P = e^{-\sqrt{AD}}$

$$P = \left(\frac{1-e^{-AD}}{AD}\right)^2$$

Width and Length Reduction

- A typical cross section of the n-channel MOSFET along EE' and FF' is compared with the ideal.

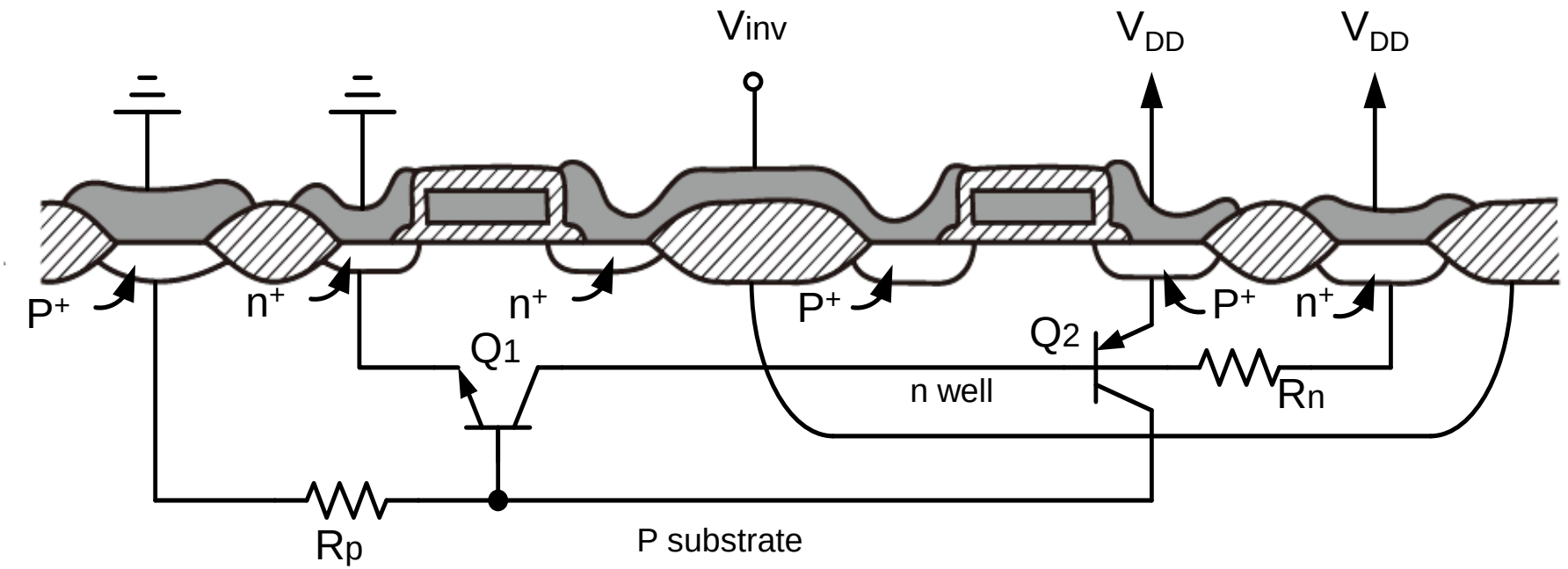


- Electric field effect due to scale down → V ↓

Latch-up

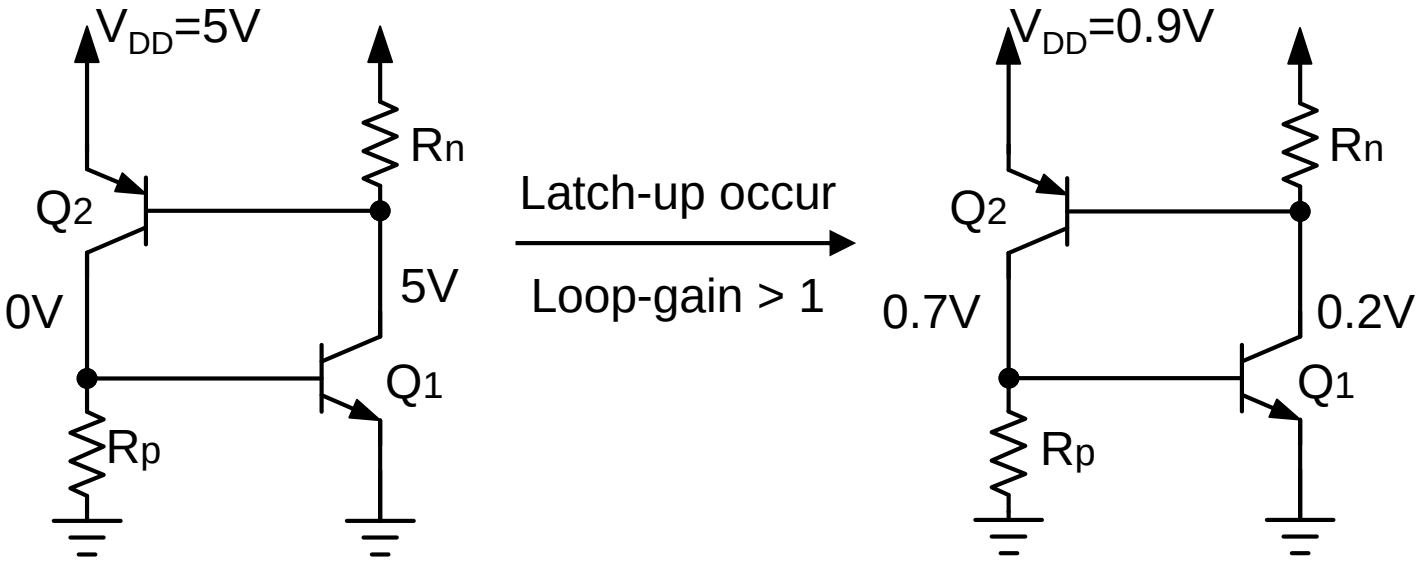
- Latch-up is a destructive phenomenon in CMOS integrated circuits
  - NPNP or PNPN structure forms a Silicon-Controlled Rectifier(SCR).
  - Occur when there are relatively large substrate or well currents
  - When latch-up occur, the circuit may be destroyed.

- Consider a CMOS inverter example shown below



Latch-up (Cont.)

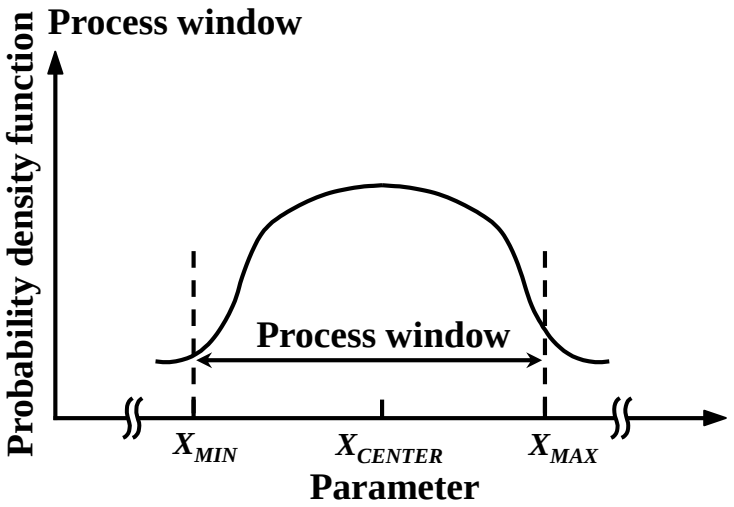
- The equivalent SCR circuit of CMOS example
  - Two cross-coupled common-emitter amplifiers
  - Positive feedback loop (Latch-up turn on when loop-gain > 1)



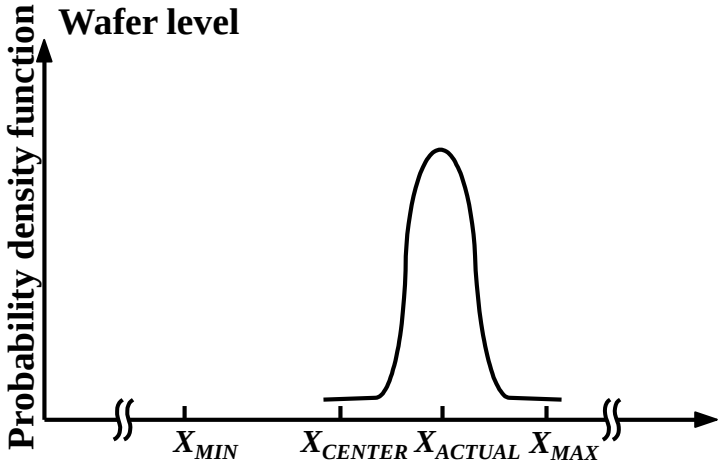
- Latch-up prevention
  - Low impendence path from V_{DD} to substrate and well (specified by design rule): R_p , R_n ↓ → Loop gain ↓
  - Use guard rings

Statistical Parameter Spreads

- Different wafers



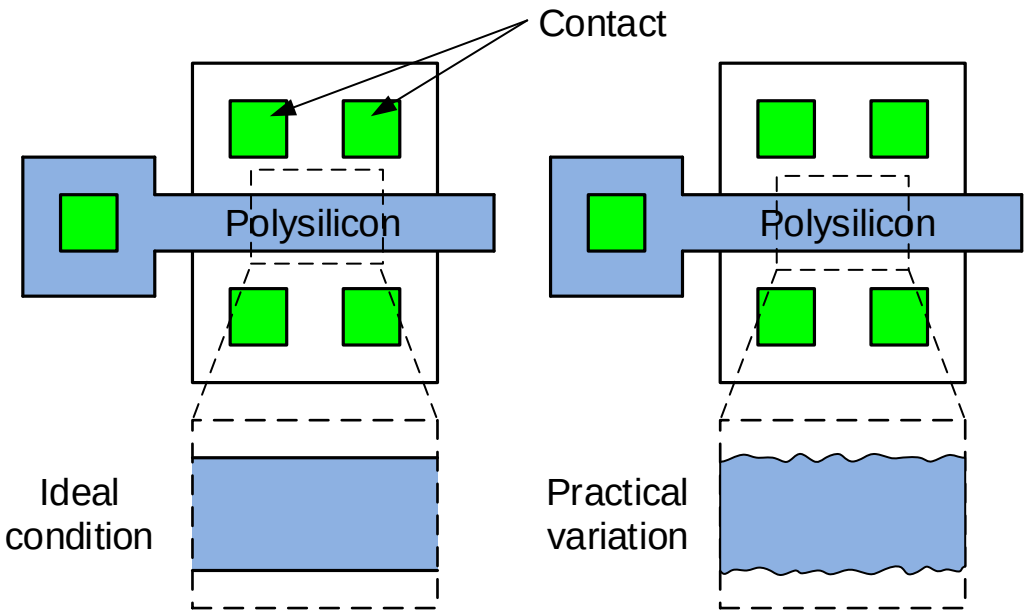
- Same wafer



- Absolute value → Poor
- Matching (or ratio) → Good

Component Accuracy

- Physical variation in a transistor



- Capacitors, resistors, transistors and dimensions, e.g. L, W, t
  - Absolute component value tolerances better than 1%(or even 10%)are not currently feasible without trimming in any IC process
  - Ratio accuracy better than 1% is achievable without trimming